

The title was objected to by the Examiner. Applicant has amended the title to be more descriptive.

Claims 1-15 were rejected under 35 U.S.C. 103(a) as unpatentable over U.S. Patent Application Publication No. 2002/0022366 A1 to Cabral, Jr. et al. (hereinafter "Cabral"), in combination with of U.S. Patent No. 5,780,889 to Hu et al. (hereinafter "Hu") and U.S. Patent Application Publication No. 2001/0029067 A1 to Hirano (hereinafter "Hirano"). The rejection is respectfully traversed.

To establish a prima facie case of obviousness, all of the following criteria should be met. First, there should be a suggestion or motivation in the art to modify the reference or to combine reference teachings. Second, there should be a reasonable expectation of success. Third, the reference(s) must teach all the claim limitations. MPEP section 706.02(j). Applicant respectfully submits that the Examiner's citations to the art are insufficient to satisfy all of the three criteria above and accordingly, the rejection should be withdrawn.

The Examiner appears to have cited Cabral as teaching a semiconductor device including a SOI film having a thickness that "is 0.003 μm or greater and 0.1 μm or smaller." Office Action at page 3. The Examiner then conceded that "Cabral, Jr. fail to teach a power supply voltage and an SOI impurity concentration." Office Action at page. 3. The Examiner then applied Hu as teaching a power supply voltage of 0.6 V. The Examiner then applied Hirano as teaching "an impurity concentration of an SOI film in the order to magnitude of $10^{17}/\text{cm}^3$." Office Action at page 3.

The Examiner concluded at page 4 of the Office Action that "it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Cabral, Jr. et al. with the power supply voltage of Hu et al. and the SOI concentration of Hirano to provide a semiconductor device capable of suppressing delay in operation."

However, the Examiner appears to have cited no portion of Hu that suggests that the use of 0.6 V in the Cabral structure will provide "a semiconductor device capable of suppressing delay in operation." Similarly, the Examiner cited no portion of Hirano that suggests that the use

of an impurity concentration of $10^{17}/\text{cm}^3$ in the Cabral structure will provide "a semiconductor device capable of suppressing delay in operation."

Applicant also notes that the Examiner did not appear to establish why one of ordinary skill would only combine certain features of the references and whether such a combination would likely be successful. For example, the Examiner cited no portion of the art that explains why one would choose to combine the specific impurity concentration cited by the Examiner in Hirano with Cabral and not also combine other features of Hirano with Cabral.

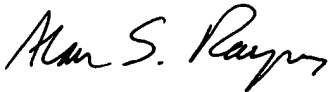
As stated in the MPEP at section 2143, "the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure." Absent evidence in the art to indicate that one of ordinary skill would have a reason (other than hindsight based on the disclosure and claims of the present application) to make the proposed combination, and evidence in the art to indicate a likelihood that that references can be successfully combined as suggested, applicant respectfully submits that the rejection should be withdrawn.

In sum, applicant respectfully submits that the Examiner has not met the proper burden to establish a suggestion or motivation in the art for the desirability of the proposed modification and combination of references. As stated by the Federal Circuit, "particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed." In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000)(emphasis added). In addition, the Examiner has not met the proper burden to establish a likelihood of success for the proposed combination. For either reason alone, the Examiner has not established a prima facie case of obviousness and the rejection should be withdrawn.

Applicant respectfully submits that claims 1-15 are in patentable form. Reexamination and reconsideration are respectfully requested. If, for any reason, the application is not in

condition for allowance, the Examiner is requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,



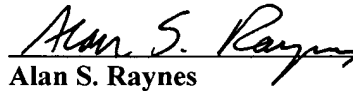
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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on March 4, 2003.

 March 4, 2003
Alan S. Raynes (Date)